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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,399	12/12/2003	Narendra V. Shenoy	SNPS-0537	1179

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EXAMINER	
PARIHAR, SUCHIN	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/734,399	SHENOY ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/12/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 11-17, 21-27 and 31-32* is/are rejected.

7)☒ Claim(s) *8-10, 18-20 and 28-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to application 10/734,399, filed 12/12/2003. Claims 1-32 are pending in this application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-7, 11-17, 21-27, 31 and 32 are rejected under 35 U.S.C. 102(e)** as being anticipated by Or-Bach (US PG Pub 2006/0176075).

3. With respect to claims 1, 11, 21, 31 and 32, Or-Bach teaches:

receiving a description of a mask-programmable cell (i.e. description of a programmable logic cell: logic cell includes at least one LUT, inputs, outputs etc., paragraph [0093]), wherein instances of the mask-programmable cell are repeated (i.e. logic cells constitute repeated subpatterns, paragraph [0091]) to form the mask-programmable fabric (array of programmable logic cells, see claim 1 of Or-Bach);

using the description of the mask-programmable cell to generate a derived library (build a library, paragraph [0577]) containing cells that can be obtained by programming the mask-programmable cell (cells can be configured to perform more than 32,000 different logic functions, paragraph [0029]);

receiving a high-level design for the integrated circuit (high level design, paragraph [0577]);

performing a synthesis operation on the high-level design (synthesize high level design, see Figure 54) to generate a preliminary netlist (produce e-NETLIST, see Figure 54) for the high-level design that contains references to cells in the derived library (produce e-NETLIST using library, see Figure 54); and

converting the preliminary netlist into a netlist (convert the design from high-level description code RTL to the level of gate netlist, paragraph [0028]) that contains references to the mask-programmable cell.

4. With respect to claims 2, 12 and 22, Or-Bach teaches all the elements of claims 1, 11 and 21, from which the claims depend respectively. Or-Bach teaches: performing a placement operation and a routing operation on the netlist to produce a layout for the integrated circuit (routing and placement of connections, paragraph [0473]; also see paragraph [0540]: discussion of the placement of cells).

5. With respect to claims 3, 13 and 23, Or-Bach teaches all the elements of claims 2, 12 and 22, from which the claims depend respectively. Or-Bach teaches: wherein performing the routing operation involves programming the mask-programmable logic ("step of programming includes programming logic functions", paragraph [0092]) and mask-programmable interconnect (programming of an integrated circuit device includes removing a portion of electrical conductive paths for selectable configuration, paragraph [0181]).

6. With respect to claims 4, 14 and 24, Or-Bach teaches all the elements of claims 1, 11 and 21, from which the claims depend respectively. Or-Bach teaches: wherein the mask-programmable logic and the mask-programmable interconnect that make up the mask-programmable fabric can be programmed by changing inter-metal via layers and/or metal layers (gate array [i.e. fabric] routing structure where the via layer and second metal layer are customized [i.e. changed, changeable], paragraph [0015]).

7. With respect to claims 5, 15 and 25, Or-Bach teaches all the elements of claims 1, 11 and 21, from which the claims depend respectively. Or-Bach teaches: wherein the method further comprises performing a packing operation on the netlist to combine cells ("e-packing", or clustering logic elements into cells, paragraph [0579]) that can use free resources from other cells.

8. With respect to claims 6, 16 and 26, Or-Bach teaches all the elements of claims 5, 15, and 25, from which the claims depend respectively. Or-Bach teaches: wherein the packing operation involves considering:

drive strengths of output pins for mask-programmable cells (discussion of drive strengths, paragraph [0522]);

routability of pins for mask-programmable cells (routing connections, paragraph [0346]);

net count for mask-programmable cells (one [i.e. a count] electrical conductive path [i.e. net], paragraph [0049]); and

active pin count for mask-programmable cells (multiplicity of inputs and outputs, see Abstract).

9. With respect to claims 7, 17 and 27, Or-Bach teaches all the elements of claims 1, 11 and 21, from which the claims depend respectively. Or-Bach teaches: wherein the mask-programmable cell includes a sequential logic portion (sequential nature of the logic, paragraph [0022]), and wherein the derived library (library functions, see paragraph [0028]) contains a sequential cell (see RAM [i.e. sequential component] block 4022 of Figure 57A), which corresponds the sequential logic portion of the mask-programmable cell (sequential nature of the logic, paragraph [0022]).

Allowable Subject Matter

10. Claims 8-10, 18-20 and 28-30 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claims 8, 18 and 28, the prior art made of record fails to teach:

wherein the description of the mask-programmable cell defines one or more pins;

wherein a pin may be specified as being tied to power, ground, a route segment or another pin;

wherein a pin may be associated with a logic function; and

wherein a pin may be specified as part of a sequential element.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suchin Parihar
Examiner
AU 2825

PAUL DINH
PRIMARY EXAMINER

Paul Dinh